AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A plasma display panel, comprising:

a first substrate;

a second substrate facing the first substrate with a discharge space therebetween;

a sealing layer located between the first substrate and the second substrate; ~~and~~

a buffer layer formed between the first substrate and the sealing layer to compensate the thermal stress of the first substrate and the sealing layer;

an upper dielectric layer formed on the first substrate; and

a protective film formed on the upper dielectric layer.

2. (Currently Amended) The plasma display panel according to claim 1, wherein the buffer layer is composed of PbO of 45~55%, ~~B2O3~~ B_2O_3 of 10~20%, ~~Al2O3~~ Al_2O_3 of 10~20% and ~~SiO2~~ SiO_2 of 15~25%.

3. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the first substrate.

4. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the first substrate.

5. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the buffer layer is different from the thermal expansion coefficient of the sealing layer.

6. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the buffer layer is the same as the thermal expansion coefficient of the sealing layer.

7. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the first substrate is around $80X10^{-7}$~$95X10^{-7}$/°C.

8. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the sealing layer is around $65X10^{-7}$~$80X10^{-7}$/°C.

9. (Original) The plasma display panel according to claim 1, wherein the thermal expansion coefficient of the buffer layer is around $72X10^{-7}$~$86X10^{-7}$/°C.

10. (Canceled)

11. (Currently Amended) The plasma display panel according to claim 1, ~~further comprising:~~

~~an~~ wherein the upper dielectric layer is formed on the ~~first substrate;~~ buffer layer and

~~a~~ the protective film is formed on the upper dielectric layer such that the buffer layer is provided between the first substrate and the upper dielectric layer and such that the upper dielectric layer is provided between the buffer layer and the protective film.

12. (Original) The plasma display panel according to claim 11, wherein the buffer layer is formed to be extended from the upper dielectric layer.

13. (Currently Amended) The plasma display panel according to claim [[12]]1, wherein the buffer layer is separately formed of a different material from the upper dielectric layer.

14-25. (Canceled)

26. (New) A plasma display panel, comprising:

a first substrate;

a second substrate arranged with respect to the first substrate such that a discharge space is provided therebetween;

a sealing layer between the first substrate and the second substrate; and

a buffer layer formed between the first substrate and the sealing layer such that the buffer layer is provided only in an area between the first substrate and the sealing layer, the buffer layer to compensate thermal stress of the first substrate and the sealing layer.

27. (New) The plasma display according to claim 26, wherein the sealing layer extends in a longitudinal direction from a first end to a second end, the first end located proximal to the first substrate and the second end located proximal to the second substrate, the buffer layer provided only in the area between the first end of the sealing layer and the first substrate.

28. (New) The plasma display according to claim 26, further comprising:

another sealing layer between the first substrate and the second substrate; and

another buffer layer formed between the first substrate and the another sealing layer such that the another buffer layer is provided only in another area between the first substrate and the another sealing layer, the another buffer layer to compensate thermal stress of the first substrate and the another sealing layer.

29. (New) The plasma display panel according to claim 28, further comprising:

an upper dielectric layer formed on the first substrate between the buffer layer and the another buffer layer; and

a protective film formed on the upper dielectric layer.

30. (New) The plasma display panel according to claim 26, wherein a thermal expansion coefficient of the buffer layer is different from a thermal expansion coefficient of the first substrate.

31. (New) The plasma display panel according to claim 26, wherein a thermal expansion coefficient of the buffer layer is different from a thermal expansion coefficient of the sealing layer.

32. (New) A plasma display comprising:

a first substrate;

a second substrate arranged with respect to the first substrate such that a discharge space is provided therebetween;

a sealing layer between the first substrate and the second substrate;

a buffer layer provided on the first substrate and provided between the first substrate and the sealing layer to compensate thermal stress of the first substrate and the sealing layer;

a dielectric layer on the buffer layer, the buffer layer being different than the dielectric layer; and

a protective film on the dielectric area such that the dielectric layer is between the buffer layer and the protective film and the buffer layer is between the first substrate and the dielectric layer.

33. (New) The plasma display panel according to claim 1, wherein the buffer layer is different than the upper dielectric layer.